REMARKS

Claims 1-15 are pending in the present application. Claims 1, 9, 13 and 14 are the independent claims. Claim 13 includes a number of means-plus-function clauses which must be given interpretations in accordance with 35 U.S.C. Section 112, ¶6. All claims stand rejected.

Claim 11 has been amended to correct an obvious typographical error, inserting a space after "claim 9."

Rejection of Claims 1-15 under 35 U.S.C. § 135(b)

Claims 1-15 have been rejected under 35 U.S.C. § 135(b) as being anticipated by Yoshimura et al. (U.S. Patent No. 5,994,934) ("Yoshimura"). Applicant respectfully traverses those rejections and requests reconsideration.

To aid in understanding the present invention, an example embodiment is described below. It will be understood that this embodiment is illustrative and is not intended to limit the scope of the invention being defined by the claims.

A prior art delay-lock loop (DLL) circuit is shown in Figs. 1 and 2. The DLL includes a voltage-controlled delay (VCD) 102 and a phase detector 104. The DLL can also be reset.

After a reset of the DLL, the VCD 102 could, for example, be reset to a minimum delay and the phase relationship between CLK_REF and CLK_FB might, for example, be such that the phase detector issues a "DOWN" command to decrease the VCD delay. In such a situation however, as a result of the VCD being already at a minimum delay, the VCD does not respond to this command. As a result, the DLL cannot achieve a "lock" between the signals.

The example phase detector 412 illustrated in Fig. 4 addresses this problem, utilizing an initialization circuit 410. After a reset at RESETb, either clock signal may be received first. However, the initialization circuit 410 disables the phase detector until the CLK_REF has been received. Further, the "DOWN" command (to decrease the delay) is disabled until the feedback clock CLK_FB has also been received. As a result, the circuit after a reset only allows an increase in delay of the VCD, and allows a decrease in delay only after this increase (Specification, page 8 lines 16-25). The illustrated initialization circuit therefore prevents the DLL from encountering a no-lock condition as described above.

Yoshimura describes a DLL circuit as shown in Fig. 9 of the reference. Here, a phase comparator 3 compares the reference clock CLKIN and the feedback clock FBCLK, and controls the delay line 9 as described above in reference to the prior art. Further, a "lock deviation judge circuit" 13 detects whether a "lock deviation phenomenon" has occurred. This phenomenon occurs when, due to changes in the circuit (e.g., temperature), the delay needed to achieve a "lock" is out of the range of the delay line 9 (Yoshimura, col. 3 lines 1-45 and Fig. 20). The delay line 9 therefore cannot synchronize the reference and feedback clocks. In response, the lock deviation judge circuit 13 causes a reset and inverts the phase of the feedback clock, as shown in Fig. 13 by signal FBCLK at time t22 (col. 12, lines 17-26). As a result, the feedback clock is adjusted so that a lock can be achieved by the delay line 9.

Yoshimura does not teach or suggest the present invention, at least because it fails to disclose an initialization circuit or method as claimed in independent claims 1, 9, 13 and 14. In Yoshimura, the "lock deviation judge circuit" 13 activates a reset signal for a predetermined period of time (col. 12 lines 64-67). While the reset is active, a second control signal at the phase comparator is forced to be inactive (col. 5 lines 54-59), and a first control signal "is outputted preferentially" (col. 5 lines 60-63). Thus, Yoshimura describes a reset operation that allows a delay in only one direction while the reset is active.

This reset operation of Yoshimura merely inactivates one phase control signal to give preference to another control signal for a predetermined period of time. In contrast, an initialization circuit as recited in the claims employs a set of conditions as previously described to ensure that the DLL circuit initially changes delay in one direction, and allows a change in an opposite direction "...after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock." Applicant's attorneys have read the alleged relevant passages referred to by the Examiner (col.4 lines 57-67 and col.5, lines 53-57) and Applicant respectfully submits that the Examiner reconsider those passages and conclude that the above-mentioned conditions are not taught by Yoshimura. Moreover, the above-mentioned conditions are superior to Yoshimura because they are not limited to a predetermined period of time, and therefore may operate more quickly than Yoshimura to change delay in a DLL circuit.

For at least the foregoing reasons, Yoshimura fails to teach the initialization circuit or method as claimed in Claims 1, 9, 13 and 14. Claims 2-8, 10-12 and 15 depend directly or indirectly from claims 1, 9 and 14 respectively, and thus the foregoing applies to these claims as well. As a result, the rejection of claims 1-15 cannot stand, and Applicant respectfully requests reconsideration.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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